In the Claims

Please cancel claims 1-20 and add new claims 21-50:

1-20.   (Cancelled)

21.   (New)   A processor comprising:

a first logic to convert a first operand from a first format into a second format; and

a second logic to combine a portion of the converted first operand with a portion of a second operand that is in the second format.

22.   (New)   The processor of claim 21, further comprising a third logic to compare a first exponent corresponding to the first operand with a second exponent of the second operand.

23.   (New)   The processor of claim 22, further comprising a fourth logic to modify a larger one of the first exponent or second exponent in accordance with the comparison.

24.   (New)   The processor of claim 22, further comprising a fourth logic to align the portion of the converted first operand and the portion of the second operand in accordance with the comparison.

25.   (New)   The processor of claim 21, wherein the second logic combines a plurality of single precision operands in a same path as a double precision exponent or a double-extended precision path.

26.   (New)   The processor of claim 21, further comprising a third logic to convert the second operand from a third format into the second format.

27.　(New)　The processor of claim 21, wherein the portion of the converted first operand or the portion of the second operand comprises a mantissa.

28.　(New)　The processor of claim 21, wherein the second logic combines the portion of the converted first operand and the portion of the second operand by an addition operation or a subtraction operation.

29.　(New)　The processor of claim 21, further comprising a third logic to normalize results of the combination by the second logic.

30.　(New)　The processor of claim 21, further comprising a third logic to round results of the combination by the second logic.

31.　(New)　The processor of claim 21, further comprising a third logic to analyze a portion of the converted first operand and the second operand to determine whether one of the first or second operands corresponds to a denormal operand.

32.　(New)　The processor of claim 21, further comprising one or more processor cores, wherein at least some of the one or more processor cores comprise one or more of the first logic or the second logic.

33.　(New)　The apparatus of claim 32, wherein at least one of the one or more processor cores, the first logic, and the second logic are on a same die.

34.　(New)　A method comprising:

　　　　modifying a plurality of operands into a same format; and

　　　　combining a plurality of mantissas corresponding to the modified plurality of operands.

35.　(New)　The method of claim 34, further comprising comparing portions of the modified plurality of operands.

36. (New) The method of claim 34, further comprising aligning portions of the plurality of mantissas.

37. (New) The method of claim 34, wherein combining the plurality of mantissas comprises adding the plurality of mantissas.

38. (New) The method of claim 34, further comprising normalizing results of the combination of the plurality of mantissas.

39. (New) The method of claim 34, further comprising rounding results of the combination of the plurality of mantissas.

40. (New) A system comprising:

a memory to store data;

a first logic to fetch an opcode, a first operand, and a second operand from the memory;

a second logic to modify the first operand and the second operand into a same format; and

a third logic to align one of the first or second operands in accordance with a comparison of a first exponent corresponding to the first operand and a second exponent corresponding to the second operand.

41. (New) The system of claim 40, further comprising a fourth logic to combine a portion of the first operand and a portion of the second operand.

42. (New) The system of claim 41, further comprising a fifth logic to normalize an output of the fourth logic.

43. (New) The system of claim 41, further comprising a fifth logic to round an output of the fourth logic.

44. (New) The system of claim 41, wherein the fourth logic combines the portion of the first operand and the portion of the second operand through an addition operation or a subtraction operation.

45. (New) The system of claim 40, further comprising a fourth logic to rotate an output of the second logic or the third logic.

46. (New) The system of claim 40, further comprising a fourth logic to analyze a portion of the first operand and the second operand to determine whether one of the first or second operands corresponds to a denormal operand.

47. (New) The system of claim 40, wherein the memory comprises one or more of a level 1 cache, a mid-level cache, or a last level cache.

48. (New) The system of claim 40, further comprising a plurality of processor cores to access the data stored in the memory.

49. (New) The system of claim 48, wherein at least one of the plurality of processor cores and the first logic are on a same die.

50. (New) The system of claim 40, further comprising an audio device.